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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

# APPLICATION FOR LETTERS PATENT

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# Method Of Forming A Thin Film Transistor

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ATTORNEY'S DOCKET NO. MI22-414

EL 844046657

1 TECHNICAL FIELD

2 This invention relates to thin film transistors and to methods of  
3 forming thin film transistors.  
4

5 BACKGROUND OF THE INVENTION

6 As circuit density continues to increase, there is a corresponding  
7 drive to produce smaller and smaller field effect transistors. Field  
8 effect transistors have typically been formed by providing active areas  
9 within a bulk substrate material or within a complementary conductivity  
10 type well formed within a bulk substrate. Although the field effect  
11 transistor feature size is reducing with advances in process technology,  
12 even greater packing density can be achieved by forming transistors in  
13 thin films deposited over insulating layers, such as oxide. These  
14 transistors are commonly referred to as "thin film transistors" (TFTs).

15 With TFTs, a thin film of semiconductive material is first  
16 provided. A central channel region of the thin film is masked, while  
17 opposing adjacent source/drain regions are doped with an appropriate p  
18 or n type conductivity enhancing impurity. A gate insulator and gate  
19 are provided either above or below the thin film channel region, thus  
20 providing a field effect transistor having an active channel region formed  
21 entirely within a thin film as opposed to a bulk substrate.

22 The invention grew out of needs associated with TFTs and their  
23 usage in high-density static random access memories (SRAMs) and flat  
24 panel displays. A static memory cell is characterized by operation in

1 one of two mutually exclusive and cell-maintaining operating states.  
2 Each operating state defines one of the two possible binary bit values,  
3 0 or 1. A static memory cell typically has an output which reflects the  
4 operating state of the memory cell. Such an output produces a "high"  
5 voltage to indicate a "set" operating state. The memory cell output  
6 produces a "low" voltage to indicate a "reset" memory cell operating  
7 state. A low or reset output voltage usually represents a binary value  
8 of 0, and a high or set output voltage represents a binary value of 1.

9 A static memory cell is said to be bi-stable because it has two  
10 stable or self-maintaining operating states, corresponding to two different  
11 output voltages. Without external stimuli, a static memory cell will  
12 operate continuously in a single one of its two operating states. It has  
13 internal feedback to maintain a stable output voltage, corresponding to  
14 operating states of the memory cell, as long as the memory cell  
15 receives power.

16 The operation of the static memory cell is in contrast to other  
17 types of memory cells, such as dynamic cells, which do not have stable  
18 operating states. A dynamic memory cell can be programmed to store  
19 a voltage which represents one of two binary values, but requires  
20 periodic reprogramming or "refreshing" to maintain this voltage for more  
21 than very short time periods. A dynamic memory cell has no feedback  
22 to maintain a stable output voltage. Without refreshing, the output of  
23 a dynamic memory cell will drift towards intermediate or indeterminate  
24 voltages, effectively resulting in loss of data.

Dynamic memory cells are used in spite of this limitation because of the significantly greater packaging densities which can be attained. For instance, a dynamic memory cell can be fabricated with a single MOSFET transistor, rather than the six transistors typically required in a static memory cell. SRAM cell density can be maximized with three-dimensional integration. For example, load transistors of the SRAM cell constitute TFTs which are folded over the bulk transistors. Because of the significantly different architectural arrangements and functional requirements of static and dynamic memory cells and circuits, static memory design has developed along a different path than has the design of dynamic memories.

Ongoing efforts in SRAM circuitry have brought about the development of TFTs in an attempt to minimize space and for other advantageous reasons associated with TFTs. While the invention grew out of needs associated with TFTs of SRAM circuitry, the artisan will appreciate applicability of the invention to other types of circuitry. By way of example only, such include TFT-based liquid crystal or other active matrix displays, where a TFT can be used as a pass transistor in a pixel element and also in the driver circuitry.

One common material utilized as the thin source, channel and drain film in a TFT is polysilicon. Such is comprised of multiple forms of individual single crystal silicon grains. The locations where two individual crystalline grains abut one another is commonly referred to as a grain boundary. Grain boundaries are inherent in polycrystalline

materials, such as polysilicon, as it is the boundaries which define the breaks between individual crystal grains. The crystalline structure breaks down at the grain boundaries, giving rise to a high concentration of broken or "dangling" Si bonds. These dangling bonds "trap" carriers and give rise to potential barriers at the grain boundaries. These potential barriers impede the flow of carriers in polysilicon, thus reducing conductivity compared to bulk silicon.

The grain boundary potential barrier height is proportional to the square of the dangling bond density, or "trap density". The smaller the grain size, the higher the trap density and thus the lower the conductance. In a TFT, the grain boundary potential barrier height in the channel is controlled by the gate voltage, and hence the conductivity is a function of the gate voltage. The TFTs, however, have a lower drive compared to bulk transistors because of lower mobility in the channel and higher threshold voltage to the larger trap concentration.

The grain boundary trap concentration also affects the leakage current of OFF-current in TFTs. In polysilicon or other polycrystalline TFTs, the presence of grain boundary traps at the drain end can dramatically increase the leakage current in the presence of a "gate-to-drain" electric field. The increase in leakage results from either "thermionic field emission" and/or "Poole-Frenkel" emission through the grain boundary traps. Accordingly, the greater the number of grain boundaries (i.e., the smaller the grain size), the greater the current leakage through the material. Greater current leakage means that more

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1 power is required to replace the leaking current to maintain an SRAM  
2 cell transistor in its desired powered-on state. Such leakage is  
3 particularly adverse in laptop computers, where desired power  
4 consumption when a cell's state is not being changed would be desired  
5 to be very low to extend battery life.

6 High density SRAMs (16 Mb or higher) typically require TFTs  
7 with low OFF currents ( $<50\text{fA}$ ) and high ON current ( $>5\text{nA}$ ) in order  
8 to obtain acceptable low standby leakage and high memory cell stability.  
9 Current state-of-the-art TFTs provide low standby current at the expense  
10 of ON current, or at the expense of additional process complexity.  
11 One present way of minimizing this current leakage at the cost of  
12 increased process complexity is by providing a "lightly doped offset"  
13 (LDO) region within the thin film. A lightly doped offset region is an  
14 elongated region within the thin film which is positioned effectively  
15 between the channel region and the drain region which is not under  
16 "direct" control of the gate fields, but rather is affected by the gate's  
17 "fringing fields". Such a region provides a buffer zone for the electric  
18 field between the channel and drain which minimizes leakage  
19 therebetween.

20 One prior art manner of contending with problems associated with  
21 grains boundaries is to "passivate" such boundaries after their formation.  
22 One technique involves exposing the thin film polycrystalline layer to  
23 atomic or plasma hydrogen, with the intent being to tie-up the dangling  
24 Si bonds at the boundaries with hydrogen. An alternate technique is

1 to implant fluorine into the thin film polycrystalline layer in an effort  
2 to produce silicon-fluorine bonds at the boundary interfaces. A  
3 silicon-fluorine bond is much more desirable than a silicon hydrogen  
4 bond due to increased high temperature stability. However, the existing  
5 ion implantation techniques of providing fluorine into a polycrystalline  
6 thin film is not without drawbacks. For example, the implantation  
7 undesirably damages the thin film layer and typically creates more  
8 dangling bonds inherent from the implantation process. Further, a large  
9 percentage of the fluorine does not reach the grain boundaries, even  
10 upon diffusion, and is therefore ineffective for the purpose of  
11 passivation, as ion implantation distributes the fluorine uniformly  
12 throughout the grains and grain boundaries.

### 13 BRIEF DESCRIPTION OF THE DRAWINGS

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15  
16 Preferred embodiments of the invention are described below with  
17 reference to the following accompanying drawings.

18 Fig. 1 is a diagrammatic sectional view of a wafer fragment at  
19 one processing step in accordance with the invention.

20 Fig. 2 is a view of the Fig. 1 wafer at a processing step  
21 subsequent to that shown by Fig. 1.

22 Fig. 3 is a view of the Fig. 1 wafer at a processing step  
23 subsequent to that shown by Fig. 2.  
24

1 Fig. 4 is a view of the Fig. 1 wafer at a processing step  
2 subsequent to that shown by Fig. 3.

3 Fig. 5 is a diagrammatic sectional view of another wafer fragment  
4 at one processing step in accordance with the invention.

5 Fig. 6 is a diagrammatic sectional view of still another wafer  
6 fragment at one processing step in accordance with the invention.

7 Fig. 7 is a view of the Fig. 6 wafer at a processing step  
8 subsequent to that shown by Fig. 6.

9 Fig. 8 is a diagrammatic sectional view of still a further wafer  
10 fragment at one processing step in accordance with the invention.

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13 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

14 This disclosure of the invention is submitted in furtherance of the  
15 constitutional purposes of the U.S. Patent Laws "to promote the  
16 progress of science and useful arts" (Article 1, Section 8).

17 In accordance with one aspect of the invention, a method of  
18 forming a thin film transistor relative to a substrate comprises the  
19 following steps:

20 providing a thin film transistor layer of polycrystalline material on  
21 a substrate, the polycrystalline material comprising grain boundaries;

22 providing a fluorine containing layer adjacent the polycrystalline  
23 thin film layer;  
24



annealing the fluorine containing layer at a temperature and for a time period which in combination are effective to drive fluorine from the fluorine containing layer into the polycrystalline thin film layer and incorporate fluorine within the grain boundaries to passivate said grain boundaries; and

providing a transistor gate operatively adjacent the thin film transistor layer.

In accordance with another aspect of the invention, a method of forming a thin film transistor relative to a substrate comprises the following steps:

providing a thin film transistor layer of polycrystalline material on a substrate, the polycrystalline material comprising grain boundaries;

providing a sacrificial fluorine containing layer over the polycrystalline thin film layer;

annealing the fluorine containing layer at a temperature and for a time period which in combination are effective to drive fluorine from the fluorine containing layer into the polycrystalline thin film layer and incorporate fluorine within the grain boundaries to passivate said grain boundaries;

after annealing, etching the sacrificial layer from the polycrystalline thin film layer; and

providing a gate dielectric layer and a gate relative to the passivated polycrystalline thin film layer.

Referring to Figs. 1-4 and initially to Fig. 1, a semiconductor wafer fragment in process is indicated generally with reference numeral 10. Such comprises a bulk substrate region 12 and an overlying insulative layer 14. A thin film transistor layer 16 of polycrystalline material is provided relative to composite substrate 12/14. Such will comprise grain boundaries inherent in polycrystalline materials. A typical and preferred material for layer 16 is polysilicon, with other polycrystalline materials, such as germanium and silicon-germanium, also being contemplated.

A fluorine containing layer 18 is provided outwardly over polycrystalline thin film layer 16. Layer 18 preferably contains such fluorine as an excess of fluorine in the form of free or loosely associated fluorine atoms. An example and preferred material for layer 18 is  $WSi_x$  provided by chemical vapor deposition utilizing  $WF_6$  and  $SiH_4$  as precursors. The fluorine from the  $WF_6$  precursor will desirably be appreciably incorporated in layer 18 for use as described below. An example process for providing layer 18 by CVD using  $WF_6$  and  $SiH_4$  in a manner which maximizes incorporated fluorine includes  $WF_6$  feed at 3 sccm, Ar at 500 sccm,  $SiH_4$  at 300 sccm, T at  $400^\circ C$  and a pressure of 1 Torr. Alternately by way of example only, fluorine containing layer 18 might predominantly comprise elemental W having incorporated fluorine, such as by utilizing a CVD process also using  $WF_6$  as a precursor. Regardless where layer 18 is to predominantly

comprise W or a W compound,  $WF_6$  is a preferred precursor for providing fluorine within such layer.

Referring to Fig. 2, wafer fragment 10 and thereby fluorine containing layer 18 is subjected to a suitable annealing temperature for a time period which in combination are effective to drive fluorine from fluorine containing layer 18 into polycrystalline thin film layer 16. Such fluorine will be incorporated within the grain boundaries to passivate said grain boundaries. The principal mechanism by which such fluorine transports from layer 18 to 16 is understood to be predominantly physical (diffusion), as opposed to by chemical action. Alternately but less preferred, such fluorine displacement from layer 18 to layer 16 might occur by a chemical mechanism. However most preferably, the annealing temperature and time are selected to be sufficiently great to drive fluorine from layer 18 into polycrystalline layer 16, but also sufficiently low to prevent a chemical reaction of layer 18 with layer 16.

For example where layer 18 predominantly comprises elemental tungsten, an annealing temperature is preferably less than  $700^\circ C$  to prevent the top or a substantial portion of layer 16 from being reacted with layer 18 to form  $WSi_x$ . Typical and example preferred annealing temperatures for a  $WSi_x$  or other as-deposited layer 18 which has reaction resistance with respect to polycrystalline material of layer 16 is from about  $600^\circ C$  to  $1000^\circ C$  for anywhere from 5 seconds (rapid thermal processing) to greater than one hour. The incorporated fluorine

1 within layer 16 preferably forms Si-F bonds with the dangling bonded  
2 silicon atoms inherent at the grain boundaries.

3 Referring to Fig. 3 and after annealing, fluorine containing  
4 layer 18 is preferably etched from outwardly of passivated polycrystalline  
5 thin film layer 16, thereby being sacrificial. An example etch chemistry  
6 where layer 18 predominately comprises  $WSi_x$  is a combination of  
7 hydrogen peroxide and ammonium hydroxide.

8 Referring to Fig. 4, subsequently a gate dielectric layer 20 is  
9 provided, along with a gate 22 outwardly relative to passivated  
10 polycrystalline thin film layer 16. Source, drain, offset,  $V_t$  adjust, or  
11 other implants would ultimately be provided to produce the desired TFT  
12 construction. Such are not shown or otherwise described, as such do  
13 not constitute aspects pertinent to the claimed invention.

14 The above described embodiment was described with reference to  
15 fluorine containing layer 18 being both sacrificial and provided after thin  
16 film transistor layer 16 was provided. Fig. 5 illustrates an alternate  
17 embodiment of a wafer fragment 10a where a fluorine containing  
18 layer 18a is neither sacrificial nor provided after provision of a thin  
19 film polycrystalline layer. Like numerals from the first described  
20 embodiment are utilized where appropriate, with differences being  
21 indicated by the suffix "a" or with different numerals. Here, fluorine  
22 containing layer 18a is provided intermediate underlying insulating  
23 layer 14 and overlying thin film polycrystalline layer 16. If fluorine  
24 containing layer 18a were electrically conductive, a fluorine transmissive

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1 electrical insulating layer (i.e., a 50 - 100 Angstroms of  $\text{SiO}_2$ ) can be  
2 provided intermediate layers 18a and 16. The selected anneal conditions  
3 (for example those described above) will effectively move fluorine atoms  
4 from layer 18a into layer 16 to provide the passivating effect.  
5 Layer 18a would then remain after passivation.

6 Another alternate embodiment wafer fragment 10b and associated  
7 processing is described with reference to Figs. 6 and 7. Like numerals  
8 from the first described embodiment are utilized where appropriate, with  
9 differences being indicated with the suffix "b" or with different numerals.  
10 Fig. 6 is of the same essential composition as the fragment of Fig. 1,  
11 but for provision of a buffering layer 25 intermediate thin film transistor  
12 layer 16 and fluorine containing layer 18. Buffering layer 25 can be  
13 provided to provide etch selectivity of layer 18 relative to 16, and as  
14 may be desired to protect the outer surface of layer 16 relative to  
15 contact with layer 18. An example and preferred material for layer 25  
16 is an insulating material, such as  $\text{SiO}_2$  deposited to a thickness of from  
17 about 50 Angstroms to about 200 Angstroms. In such instance however,  
18 buffering layer 25 will be transmissive of fluorine atoms from fluorine  
19 containing layer 18 during the annealing step.

20 Referring to Fig. 7, fluorine containing layer is illustrated as  
21 having been selectively etched relative to buffering layer 25 after driving  
22 of the fluorine atoms into layer 16. Buffering layer 25 would typically  
23 subsequently be etched, and processing continuing to occur as shown by  
24 Fig. 4 to produce a thin film transistor construction.

1 The above described embodiments were with respect to a top-  
2 gated thin film transistor construction. Fig. 8 illustrates yet another  
3 alternate embodiment whereby a bottom-gated thin film construction is  
4 provided. Like numerals from the first described embodiment are  
5 utilized where appropriate, with differences being indicated by the suffix  
6 "c" or with different numerals. Here, wafer fragment 10c is illustrated  
7 as having a bottom gate 22c provided relative to an insulating layer 27,  
8 such as  $\text{SiO}_2$ . Gate dielectric layer 20c and thin film transistor  
9 layer 16c are provided outwardly relative to layer 27 and gate 22c. A  
10 fluorine containing layer 18 is provided outwardly of polycrystalline thin  
11 film layer 16c for the annealing step. Also, a buffering layer could be  
12 provided intermediate thin film transistor layer 16c and fluorine  
13 containing layer 18.

14 Regardless and in all of the above described embodiments, a  
15 fluorine containing layer is provided operatively adjacent a polycrystalline  
16 thin film layer in a manner effective to enable an effective annealing  
17 temperature and time to transfer fluorine atoms from the fluorine  
18 containing layer to the polycrystalline thin film layer. Further and  
19 regardless, in each of the above embodiments at some point a transistor  
20 gate is provided operatively adjacent the thin film transistor layer.  
21 Further, subsequent hydrogen passivation could also be conducted without  
22 departing from the principals and scope of the invention.

23 Thin film transistors produced according to the above described  
24 embodiment have improved operating characteristics.

1 In compliance with the statute, the invention has been described  
2 in language more or less specific as to structural and methodical  
3 features. It is to be understood, however, that the invention is not  
4 limited to the specific features shown and described, since the means  
5 herein disclosed comprise preferred forms of putting the invention into  
6 effect. The invention is, therefore, claimed in any of its forms or  
7 modifications within the proper scope of the appended claims  
8 appropriately interpreted in accordance with the doctrine of equivalents.  
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